REMARKS

In response to the Official Action:

[1] Claims 1, 3, 5, and 6 are rejected under § 103 over Nakamigawa JP '556 in view of Hirano US '749. This rejection is respectfully traversed.

Electrode Posts. The Applicant's claim 1 recites "a plurality of electrode posts" and their connection to the claimed wiring patterns and the claimed external terminals. (The Applicant's electrode posts are exemplified by feature 46 in Fig. 2.) However, neither one of the applied references discloses any such electrode posts. Therefore, no combination of the references (not admitted obvious) could reach the instant claims.

The Examiner has not mentioned the electrode posts in the rejection and has not asserted that any feature of the prior art anticipates the claimed electrode posts.

Furthermore, there is no apparent reason why electrode posts should have been added to Nakamigawa, even if the prior art had disclosed them. Nakamigawa teaches preventing warp/deformation of its substrate 2 (Abstract), and thereby preventing breaks between the solder bumps 12 and a circuit board (not shown in figure next to Abstract). There is no apparent reason why adding electrode posts, which entail additional metal-metal contacts, would have helped to achieve the object of Nakamigawa.

Hirano, not based on the WCSP technique described by the Applicant's specification, and it uses fine conductive wires 10 to connect the chip and the wiring 3. Electrode posts could not be added to Hirano in any functional way—they would be redundant extra pieces if so added, and would hinder the function of Hirano. Therefore, Hirano inherently teaches against the use of electrode posts.

In sum, there is no disclosure of electrode posts in the applied art, no teaching toward electrode posts, and no advantage to be gained from electrode posts. Even if combined (not admitted), the two references would not reach the claims.

Motivation. As noted above, Hirano connects to the chip with fine wires 10. Hirano calls this a "face up design" and states that it is the most popular design because it is inexpensive

(col. 1, line 21). Hirano also states that its "invention [is] effective when used [in] a face up structure" (col. 1, line 9, Field of the Invention), and further states, at the beginning of its Summary of the Invention, that its "inventors have investigated the ... face up structure and found the below-described problems" (col. 1, line 58). The described problems are intended to be solved by the invention (col. 2, lines 36-46). Hirano defines the "face up structure" at col. 1, lines 22-51, stating that it includes a wire between the chip electrode and interconnection pad.

By limiting itself to solving problems of the face up design, Hirano directly implies that its teachings are not applicable to face *down* designs, like that of Nakamigawa. The person of ordinary skill, who was considering a modification of Nakamigawa (not admitted), would not have read past the first page of Hirano because Hirano teaches on that first page that it is applicable to a face up design, not a face down design.

This is even more true, because the person of ordinary skill also would have seen on its first page that Hirano is only concerned with reducing the length of the fine wires, in order to prevent sagging and increased inductance (col. 2). Sagging is irrelevant to Nakamigawa, and Nakamigawa discloses both lesser (Fig. 3) and greater (Fig. 4) distances between its chip electrodes 10 and solder balls 12, which arguably implies a lack of concern with inductance. Since Nakamigawa doesn't seem to need reduced inductance, and Hirano's teachings for that purpose are only relevant to fine wires not found in Nakamigawa, the person of ordinary skill would have seen no reason to proceed. Therefore, the asserted combination is not predictable from the applied prior art.

The Applicant's points (1)-(3) of August, 2006, concerning motivation, are respectfully reiterated. The Examiner has not rebutted these arguments.

[3-4] Claim 4 is rejected under § 103 over Nakamigawa in view of Hirano and Jackson US '930. This rejection is respectfully traversed on the grounds set out previously and the dependence of claim 4.

[5] Claim 7 is rejected under § 103 over Nakamigawa in view of Hirano and Torres US '213. This rejection is respectfully traversed on the grounds set out previously and the dependence of claim 7.

The Examiner has not rebutted the Applicant's earlier arguments, or answered the argument that the Examiner has misconstrued the applied 'A' and 'B' as boundaries. (The Applicant argued that these are actually radii, and invited the Examiner to note col. 3, line 61, where A' and B' are named "axis" and col. 3, line 66, stating "axis 'A' and axis 'B' may define an arc of varying radius." The Applicant asserted that there is no mention of any boundary, and that the Examiner had misconstrued the lines indicating the arcs.)

Withdrawal of the rejection is requested.

[6] Claims 8 and 9 were rejected under § 103 over Nakamigawa in view of Hirano and Ma US '469. This rejection is respectfully traversed on the grounds set out previously and the dependence of the claims.

The Applicant argued previously that the Examiner had not explained how the materials 118 and 112 of Ma were to be applied to the other two references; and that since Nakamigawa is the base reference, the Applicant had assumed that Ma was applied to it: but asked, to which layers? The Applicant noted that Nakamigawa's Abstract discloses that layer 21 is of resin, but not the extension section 9. The Applicant asserted that, because the goal of Nakamigawa is to avoid strain ("warp/deformation"), using materials of different shrinkage would be contrary to this reference. The Applicant noted that the reference does not disclose two materials with different molding shrinkage. Only resin has molding shrinkage; silicon nitride and silicon dioxide do not, because they are crystalline and never are molded. The Applicant also asserted that the specific features of claim 9 are not disclosed, but that the Examiner had asserted that these features would be obvious for "adequate mechanical rigidity, ... protection for the semiconductor chip, and ... surface area," but noted that none of these asserted advantages had been related to the coefficient of thermal expansion; and asserted that, as to the modulus of elasticity, there is no direct correlation or any reasoned argument, as required by the MPEP.

The Examiner has not rebutted or addressed these arguments.

Withdrawal of the rejection is requested.

In view of the present amendments, withdrawal of the rejections and allowance are requested.

Respectfully submitted,

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